

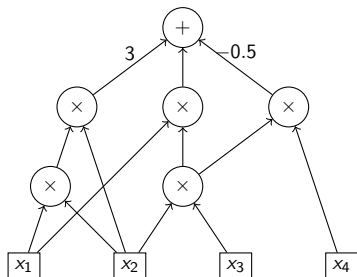
# Hitting Sets for *UPT* Circuits

Ramprasad Saptharishi and Anamay Tengse

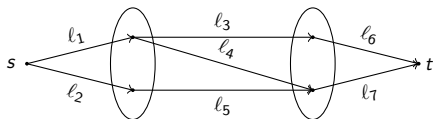
TIFR, Mumbai, India

6th March 2018

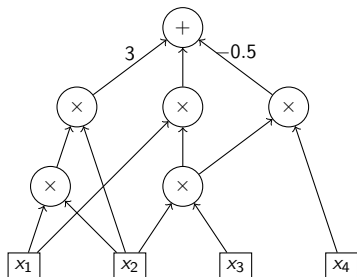
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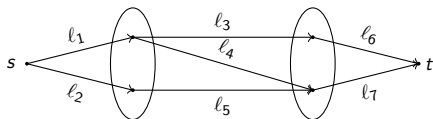
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- ▶ Introduced by Nisan [N91]
- ▶ Circuits:  
No. of nodes
- ▶ ABPs:  
Width, No. of layers



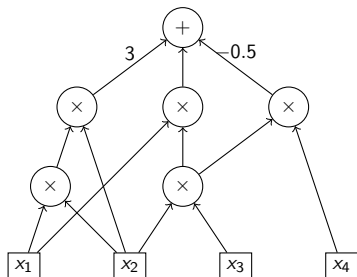
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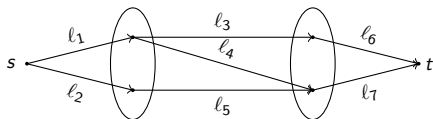
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Homogeneous circuits: Each gate is homogeneous

Homogeneous ABPs: Each of the  $l_i$ s are homogeneous

# Hitting sets for Non-commutative circuits

Given a non-commutative circuit class  $\mathcal{C} \subseteq \mathbb{F}\langle \mathbf{x} \rangle$ , a set of *matrices*  $\mathcal{H}$  is called a hitting set for  $\mathcal{C}$  if a nonzero  $C \in \mathcal{C}$  evaluates to a nonzero value on at least one input from  $\mathcal{H}$ .

**Note:** Variables from  $\mathbf{x}$  can be thought of as matrices with commuting variables from  $\mathbf{y}$  as entries.

**Strategy:** Substitute univariates of low degree, interpolate.

$$\phi : \mathbf{y} \rightarrow \mathbb{F}[t].$$

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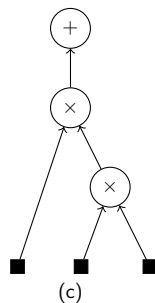
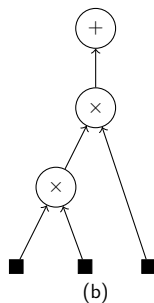
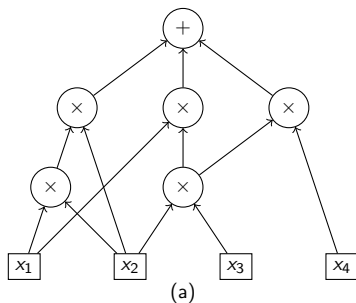
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For this talk:

- ▶ Non-commutative circuits, ABPs
- ▶ WLOG models will be homogeneous

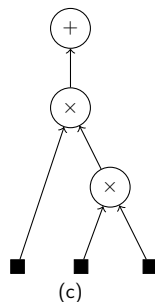
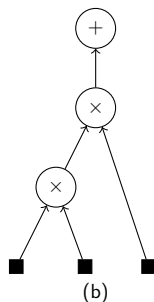
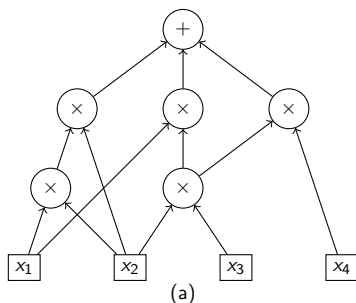
# Parse Trees and Unambiguity

Parse tree: Start from root, one child of  $+$ , all children of  $\times$



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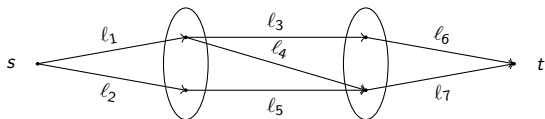
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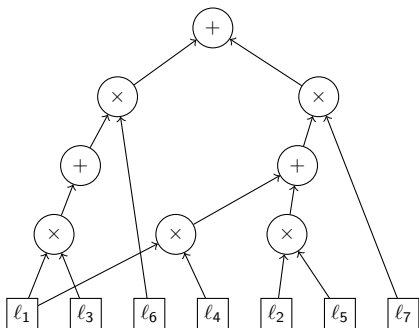
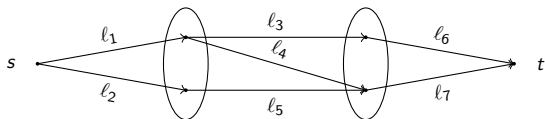
- ▶ Unambiguous or Unique Parse Tree (UPT) [LMP16]  
all parse trees have the same shape.
- ▶ ABPs  $\subsetneq$  UPT  $\subsetneq$  Circuits [LMP16]



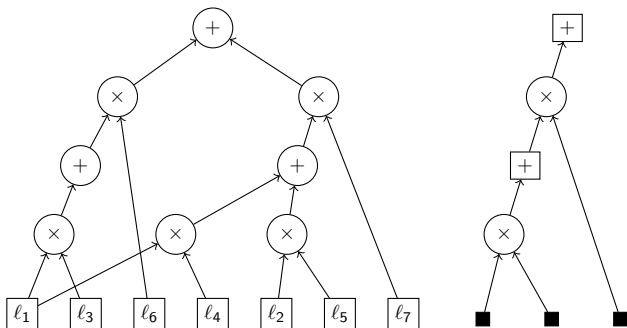
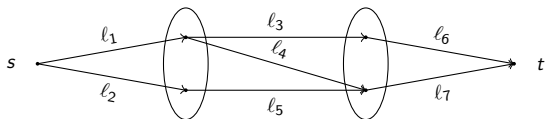
## ABPs as UPT circuits



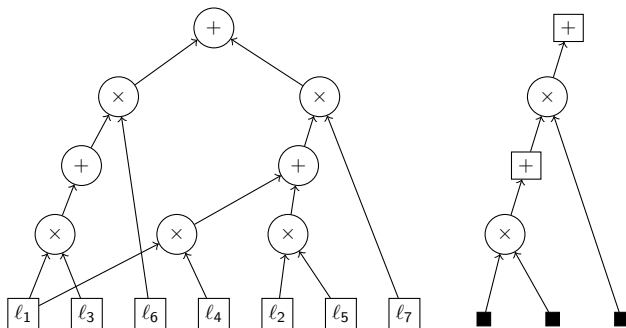
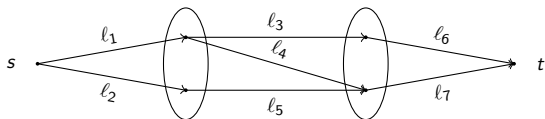
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- ▶ ABPs are UPT circuits with *left-skew* tree.

## Properties of UPT circuits [LMP16]

1. WLOG each gate appears in a fixed position in the tree.  
Can be done with a  $d$  blow-up.
2. Natural notion of *width* of a position.  
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## Plan:

- ▶ Overview of hitting sets for ABPs.
- ▶ Extend ideas to UPT circuits.

## Quick survey

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- ▶ [LMP16] introduced UPT circuits
  - ▶ Extend Nisan's characterization
  - ▶ *White box* in  $\text{poly}(n)$

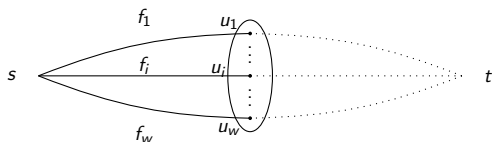
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- ▶ [LMP16] introduced UPT circuits
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  - ▶ *White box* in  $\text{poly}(n)$
- ▶ [LLS17] extend *white box* results of [GKST15].
- ▶ *This work*: BIWA for UPT circuits, extends hitting sets of [AGKS15,GKST15,GKS15].

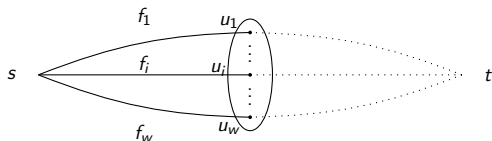
## Coefficient span [RS05,FS13]



Preserve nonzeroness of an arbitrary linear combination of  $f_i$ s.

$$M_f = \begin{bmatrix} \leftarrow & f_1 & \rightarrow \\ \leftarrow & \vdots & \rightarrow \\ \leftarrow & f_w & \rightarrow \end{bmatrix} \in \mathbb{F}[\mathbf{y}]^k \equiv \mathbb{F}^k[\mathbf{y}]$$

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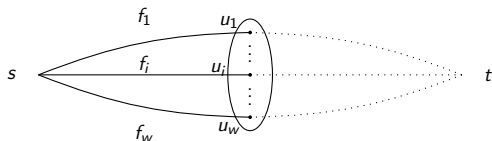
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Consider  $\phi : \mathbf{y} \rightarrow \mathbb{F}[t_1, \dots, t_k]$  ( $k \sim \log n$ )

Such a  $\phi$  sends columns of  $M_f$  to  $n^{O(k)}$  columns.



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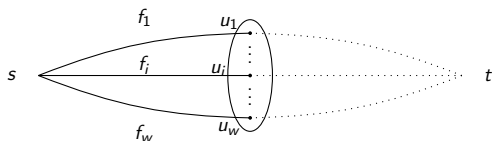
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[FS13] A  $\phi$  that preserves  $\text{colSpan}(M_f)$  suffices.

$$\text{ColSpan}(M_f) = \text{CoeffSpan}(f_1, \dots, f_w)$$

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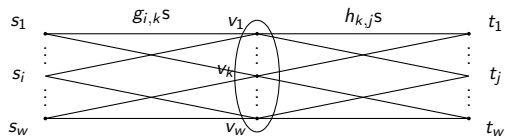
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Let  $(wt_1, \dots, wt_k) : \mathbf{y} \rightarrow [N]^k$  and  $\phi_{wt}$  be such that  
 $\phi_{wt} : y_i \mapsto t_1^{wt_1(y_i)} \dots t_k^{wt_k(y_i)}$ .

[AGKS15] If  $wt$  is a basis isolating weight assignment (BIWA) for  $M_f$ , then  $\phi_{wt}$  will preserve  $\text{CoeffSpan}$ .

How do we construct a BIWA?

# Basis Isolation [AGKS15]


 $M_f$ 

$$\begin{bmatrix} \leftarrow & f_{1,1} & \rightarrow \\ \leftarrow & \vdots & \rightarrow \\ \leftarrow & f_{w,w} & \rightarrow \end{bmatrix}$$

 $M_g$ 

$$\begin{bmatrix} \leftarrow & g_{1,1} & \rightarrow \\ \leftarrow & \vdots & \rightarrow \\ \leftarrow & g_{w,w} & \rightarrow \end{bmatrix}$$

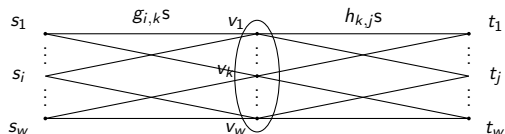
 $M_h$ 

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Define  $V_f, V_g, V_h,$

where  $V_* = \text{rowSpan}(M_*)$ .

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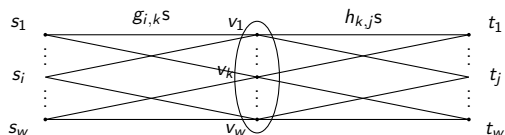


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 M_f & & M_g & & M_h \\
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Define  $V_f, V_g, V_h$ , where  $V_* = \text{rowSpan}(M_*)$ .

$$f_{i,j} = \sum_{k \in [w]} g_{i,k} h_{k,j} \in V_f \subseteq V_g \otimes V_h$$

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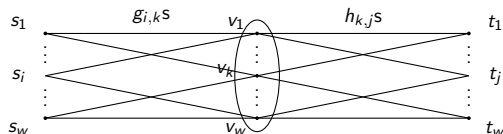


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BIWA [AGKS15]:

If  $\mathbf{wt} : \mathbf{y} \rightarrow [N]^k$  is a BIWA for  $V_g$  and  $V_h$ , then poly( $n$ ) time construction for  $\mathbf{wt}' : \mathbf{y} \rightarrow [N]$  such that  $(\mathbf{wt}, \mathbf{wt}') : \mathbf{y} \rightarrow [N]^{k+1}$  is a BIWA for  $V_f$ .

## So far...

### Abstract view of [AGKS15]

- ▶ Each layer segment with  $w^2$  edges naturally yields a vector space.
- ▶ Space  $V_f$  resulting from paths across consecutive layers  $(V_g, V_h)$  satisfies  $V_f \subseteq V_g \otimes V_h$ .
- ▶ BIWA for  $V_g$  and  $V_h$  can be extended to a BIWA for  $V_f$  by adding an extra coordinate, in  $\text{poly}(n)$  time.

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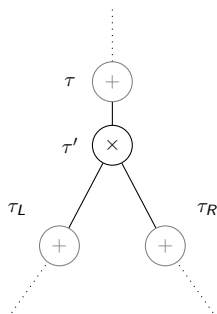
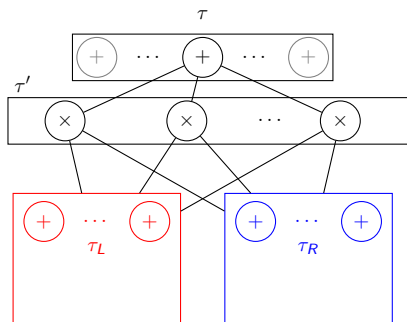
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### Properties of UPT circuits

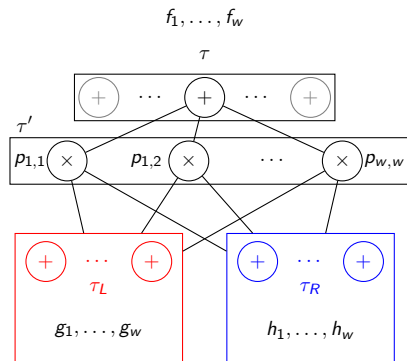
- ▶ All parse trees have the same shape, each gate  $\sim$  node.
- ▶ Analogous notion of *width* for nodes.
- ▶ All product gates are position disjoint.



# Extending AGKS to UPT ckts

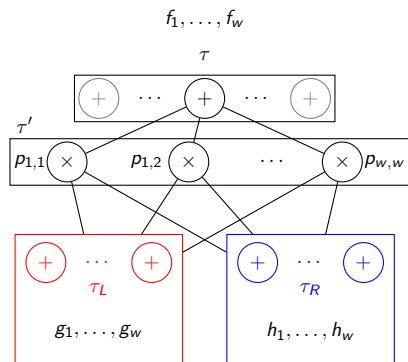


# Extending AGKS to UPT ckts



$$\rho_{i,j} = g_i \times h_j$$
$$f_k \in \langle \{g_i \times h_j : (i,j) \in [w]^2\} \rangle$$

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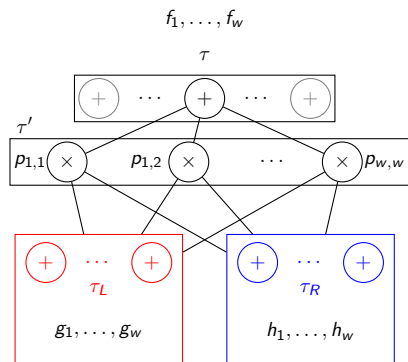
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$$V_{\tau} \equiv \begin{bmatrix} \leftarrow & f_1 & \rightarrow \\ & \vdots & \\ \leftarrow & f_w & \rightarrow \end{bmatrix}$$

$$V_{\tau'}, V_{\tau_L}, V_{\tau_R}.$$

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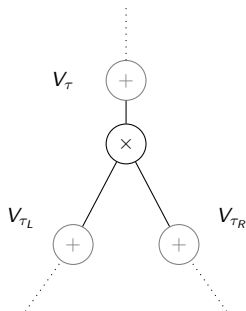
$$V_T \equiv \begin{bmatrix} \leftarrow & f_1 & \rightarrow \\ & \vdots & \\ \leftarrow & f_w & \rightarrow \end{bmatrix}$$

$$V_{T'}, V_{T_L}, V_{T_R}$$

$$V_T \subseteq V_{T'} \quad V_{T'} = V_{T_L} \otimes V_{T_R}$$

$$V_T \subseteq V_{T_L} \otimes V_{T_R}$$

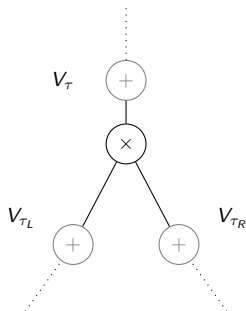
## BIWA for UPT circuits



### Lemma [AGKS15]

If  $(wt_1, \dots, wt_k)$  is a BIWA for both  $V_{T_L}$  and  $V_{T_R}$ , then in  $\text{poly}(n)$  time we can find  $wt_{k+1}$  such that  $(wt_1, \dots, wt_{k+1})$  is a BIWA for all  $V_T$ .

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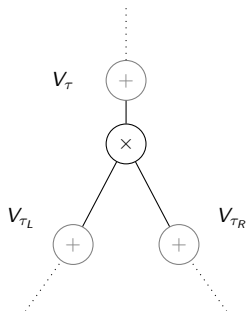


### Lemma [AGKS15]

If  $(wt_1, \dots, wt_k)$  is a BIWA for both  $V_{T_L}$  and  $V_{T_R}$ , then in  $\text{poly}(n)$  time we can find  $wt_{k+1}$  such that  $(wt_1, \dots, wt_{k+1})$  is a BIWA for all  $V_T$ .

BIWA for  $V_{\text{root}}$  with at most as many coordinates as  $\text{depth}(C)$ .

# BIWA for UPT circuits



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## Depth Reduction by *shuffling*

For every UPT  $C$  of degree  $d$ , an *equivalent* UPT  $\sigma(C)$  of depth  $O(\log d)$  exists.

## Concluding remarks

Not covered:

- ▶ Extending hitting sets for sum of  $c$  ROABPs [GKST15] and constant *width* ROABPs [GKS16] to UPT circuits.
- ▶ Exponential lower bound against UPT circuits under *shufflings* for the *moving pallindrome* defined in [LMP16].
- ▶ Quasipolynomial (tight) separation between ABPs and UPT circuits under *shufflings*, extension of [HY16].



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Thank you.